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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No.	042390.P9557
First Inventor or Application Identifier	Chun Mu
Title	PROCESS FOR FORMING A DIRECT BUILD-UP LAYER ON AN...
Express Mail Label No.	EL034437753US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

jc658 U.S. PTO 09/661899 09/14/00

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification [*Total Pages* 24]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 22]

4. Oath or Declaration [*Total Pages* 4]
a. ☐ Newly executed (original copy)
b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))

8. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☒ Power of Attorney

9. ☐ English Translation Document *(if applicable)*

10. ☐ Information Disclosure Statement (IDS)/PTO - 1449 ☐ Copies of IDS Citations

11. ☐ Preliminary Amendment

12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

13. ☐ *Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired

14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)

15. ☒ Other: CHECK FOR $924.00

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16. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: _____
Prior application Information: Examiner _____ *Group/Art Unit:* _____

For CONTINUATION or DIVISIONAL APPS only The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts

17. CORRESPONDENCE ADDRESS

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Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, Seventh Floor				
City	Los Angeles	*State*	California	*Zip Code*	90025
Country	U.S.A.	*Telephone*	(503) 684-6200	*Fax*	(503) 684-3245

Name (Print/Type)	Paul A. Mendonsa, Reg. No. 42,879		
Signature	Paul A. Mendonsa	*Date*	09/14/00

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Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.
See 37 C.F.R §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 924.00

Complete if Known	
Application Number	
Filing Date	September 14, 2000
First Named Inventor	Chun Mu
Examiner Name	
Group/Art Unit	
Attorney Docket No.	042390.P9557

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees
2. ☒ The Commissioner is hereby authorized to credit any over payments to:

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Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

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2. ☒ Payment Enclosed:
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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	$690.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

				Extra Claims		Fee from below		Fee Paid
Total Claims	33	- 20 =	13	X	18.00	=	$234.00
Independent Claims	3	- 3 =	0	X	78.00	=	
Multiple Dependent						=	

**or number previously paid, if greater, For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple Dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 234.00

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	*Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	*Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,210	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____
Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

				Complete (if applicable)	
Typed or Printed Name	Paul A. Mendonsa			Reg. Number	42,879
Signature	Paul A. Mendonsa	Date	09/14/00	Deposit Account User ID	02-2666

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PATENT
Ref. No. P9557

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APPLICATION FOR UNITED STATES PATENT

FOR

PROCESS FOR FORMING A DIRECT BUILD-UP LAYER ON AN ENCAPSULATED DIE PACKAGE AND INTERMEDIATE STRUCTURES FORMED THEREWITH

Inventors:

Qing Ma
Chun Mu
Quat T. Vu
Steven Towle

Prepared by:
Robert G. Winkle, Esq.
Reg. No. 37,474
Intel Legal Team

PROCESS FOR FORMING A DIRECT BUILD-UP LAYER ON AN ENCAPSULATED DIE PACKAGE AND INTERMEDIATE STRUCTURES FORMED THEREWITH

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to apparatus and processes for packaging microelectronic dice. In particular, the present invention relates to a packaging technology that fabricates build-up layers on a microelectronic die and on a packaging material that is adjacent the microelectronic die.

State of the Art: Higher performance, lower cost, increased miniaturization of integrated circuit components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. As these goals are achieved, microelectronic dice become smaller. Of course, the goal of greater packaging density requires that the entire microelectronic die package be equal to or only slightly larger (about 10% to 30%) than the size of the microelectronic die itself. Such microelectronic die packaging is called a "chip scale packaging" or "CSP".

As shown in FIG. 9, true CSP would involve fabricating build-up layers directly on an active surface 204 of a microelectronic die 202. The build-up layers may include a dielectric layer 206 disposed on the microelectronic die active surface 204. Conductive traces 208 may be formed on the dielectric layer 206, wherein a portion of each conductive trace 208 contacts at least one contact 212 on the microelectronic die active surface 204. External contacts, such as solder balls or conductive pins for contact with an external component (not shown), may be fabricated to electrically contact at least one conductive trace 208. FIG. 9 illustrates the external contacts as solder balls 214 which are surrounded by a solder mask material 216 on the dielectric

layer 206. However in such true CSP, the surface area provided by the microelectronic die active surface 204 generally does not provide enough surface for all of the external contacts needed to contact the external component (not shown) for certain types of microelectronic dice (e.g., logic).

Additional surface area can be provided through the use of an interposer, such as a substrate (substantially rigid material) or a flex component (substantially flexible material). FIG. 1 illustrates a substrate interposer 222 having a microelectronic die 224 attached to and in electrical contact with a first surface 226 of the substrate interposer 222 through small solder balls 228. The small solder balls 228 extend between contacts 232 on the microelectronic die 224 and conductive traces 234 on the substrate interposer first surface 226. The conductive traces 234 are in discrete electrical contact with bond pads 236 on a second surface 238 of the substrate interposer 222 through vias 242 that extend through the substrate interposer 222. External contacts 244 (shown as solder balls) are formed on the bond pads 236. The external contacts 244 are utilized to achieve electrical communication between the microelectronic die 224 and an external electrical system (not shown).

The use of the substrate interposer 222 requires number of processing steps. These processing steps increase the cost of the package. Additionally, even the use of the small solder balls 228 presents crowding problems which can result in shorting between the small solder balls 228 and can present difficulties in inserting underfilling between the microelectronic die 224 and the substrate interposer 222 to prevent contamination and provide mechanical stability.

FIG. 11 illustrates a flex component interposer 252 wherein an active surface 254 of a microelectronic die 256 is attached to a first surface 258 of the flex component interposer 252 with a layer of adhesive 262. The microelectronic die 256 is encapsulated in an encapsulation material 264. Openings are formed in the flex component interposer 252 by laser abalation through the flex component interposer 252 to contacts 266 on the microelectronic die active surface 254 and to selected metal pads 268 residing within the flex component interposer 252. A conductive material layer is formed over a second surface 272 of the flex component interposer 252 and in the openings. The conductive material layer is patterned with standard photomask/etch processes to form conductive vias 274 and conductive traces 276. External contacts are formed on the conductive traces 276 (shown as solder balls 278 surrounded by a solder mask material 282 proximate the conductive traces 276).

The use of a flex component interposer 252 requires gluing material layers which form the flex component interposer 252 and requires gluing the flex component interposer 252 to the microelectronic die 256. These gluing processes are relatively difficult and may increase the cost of the package. Furthermore, the resulting packages have been found to have poor reliability.

Therefore, it would be advantageous to develop new apparatus and techniques to provide additional surface area to form traces for use in CSP applications, while utilizing commercially available, widely practiced semiconductor fabrication techniques.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGs. 1a-1j are side cross-sectional views of a first embodiment of a process of forming a microelectronic package, according to the present invention;

FIG. 2 is a side cross-sectional view of an embodiment of a microelectronic assembly that includes a plurality of microelectronic dice, according to the present invention;

FIG. 3 is a side cross-sectional view of another embodiment of a microelectronic assembly that includes a plurality of microelectronic dice, according to the present invention;

FIG. 4 is a side cross-sectional view of still another embodiment of a microelectronic assembly that includes a plurality of microelectronic dice, according to the present invention;

FIG. 5 is a side cross-sectional view of yet another embodiment of a microelectronic assembly that includes a plurality of microelectronic dice, according to the present invention;

FIGs. 6a-6c are side cross-sectional views of a layering method for forming microelectronic packages, according to the present invention;

FIG. 7 is a top plan view of a patterned adhesive layer on a microelectronic assembly, according to the present invention;

FIG. 8 is a top plan view of an alternate patterned adhesive layer on a microelectronic assembly, according to the present invention;

FIG. 9 is a cross-sectional view of a true CSP of a microelectronic device, as known in the art;

FIG. 10 is a cross-sectional view of a CSP of a microelectronic device utilizing a substrate interposer, as known in the art; and

FIG. 11 is a cross-sectional view of a CSP of a microelectronic device utilizing a flex component interposer, as known in the art.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Although FIGs. 1a-1j and 2-8 illustrate various views of the present invention, these figures are not meant to portray microelectronic assemblies in precise detail. Rather, these figures illustrate microelectronic assemblies in a manner to more clearly convey the concepts of the present invention. Additionally, elements common between the figures retain the same numeric designation.

The present invention includes a packaging technology that fabricates build-up layers on an encapsulated microelectronic die that has expanded area larger than that of the microelectronic die. FIGs. 1a-1j illustrate a first embodiment of a process of forming a microelectronic package of the present invention. As shown in FIG. 1a, a protective film 104 is abutted against an active surface 106 of a microelectronic die 102 to protect the microelectronic die active surface 106 from any contaminants. The microelectronic die active surface 106 has at least one contact 108 disposed thereon. The contacts 108 are in electrical contact with integrated circuitry (not shown) within

the microelectronic die 102. The protective film 104 is preferably a substantially flexible material, such as Kapton® polyimide film (E. I. du Pont de Nemours and Company, Wilmington, Delaware), but may be made of any appropriate material, including metallic films. The protective film 104 may have a weak, thermally stable adhesive, such as silicone, which attaches to the microelectronic die active surface 106. This adhesive-type film may be applied prior to placing the microelectronic die 102 in a mold or other such equipment used for the encapsulation process. The protective film 104 may also be a non-adhesive film, such as a ETFE (ethylene - tetrafluoroethylene) or Teflon® film, which is held on the microelectronic die active surface 106 by an inner surface of the mold or other such equipment during the encapsulation process.

The microelectronic die 102 is then encapsulated with an encapsulation material 112, such as plastics, resins, epoxies, and the like, as shown in FIG. 1b, that covers a back surface 114 and side(s) 116 of the microelectronic die 102. The encapsulation of the microelectronic die 102 may be achieved by any known process, including but not limited to transfer and compression molding, and dispensing. The encapsulation material 112 provides mechanical rigidity, protects the microelectronic die 102 from contaminants, and provides surface area for the build-up of trace layers.

After encapsulation, the protective film 104 is removed, as shown in FIG. 1c, to expose the microelectronic die active surface 106. As also shown in FIG. 1c, the encapsulation material 112 is preferably molded to form at least one surface 110 which is substantially planar to the microelectronic die active surface 106. The encapsulation material surface 110 and the microelectronic die active surface 106 constitute the active surface 120 of the encapsulated microelectronic die assembly, which will be utilized in

further fabrication steps as additional surface area for the formation of build-up layers, such as dielectric material layers and conductive traces. The surface of the encapsulation material 112 which opposes encapsulation material surface 110 comprises at least a portion of a back surface 130 of the microelectronic die assembly.

A first dielectric layer 118, such as epoxy resin, polyimide, bisbenzocyclobutene, and the like, is disposed over the microelectronic die active surface 106, the contacts 108, and the encapsulant material surface 110, as shown in FIG. 1d. The dielectric layers of the present invention are preferably filled epoxy resins available from Ibiden U.S.A. Corp., Santa Clara, California, U.S.A. and Ajinomoto U.S.A., Inc., Paramus, New Jersey, U.S.A. The formation of the first dielectric layer 118 may be achieved by any known process, including but not limited to film lamination, spin coating, roll-coating, and spray-on deposition.

As shown in FIG. 1e, a plurality of vias 122 are then formed through the first dielectric layer 118. The plurality of vias 122 may be formed any method known in the art, including but not limited to laser drilling, photolithography, and, if the first dielectric layer 118 is photoactive, forming the plurality of vias 122 in the same manner that a photoresist mask is made in a photolithographic process, as known in the art.

A plurality of conductive traces 124 is formed on the first dielectric layer 118, as shown in FIG. 1f, wherein a portion of each of the plurality of conductive trace 124 extends into at least one of said plurality of vias 122 (see FIG. 1e) to make electrical contact therewith. The plurality of conductive traces 124 may be made of any applicable conductive material, such as copper, aluminum, and alloys thereof. As

shown in FIG. 1f, at least one conductive trace extends adjacent the microelectronic die active surface 106 and adjacent said encapsulation material surface 110.

The plurality of conductive traces 124 may be formed by any known technique, including but not limited to semi-additive plating and photolithographic techniques. An exemplary semi-additive plating technique can involve depositing a seed layer, such as sputter-deposited or electroless-deposited metal on the first dielectric layer 118. A resist layer is then patterned on the seed layer, such as a titanium/copper alloy, followed by electrolytic plating of a layer of metal, such as copper, on the seed layer exposed by open areas in the patterned resist layer. The patterned resist layer is stripped and portions of the seed layer not having the layer of metal plated thereon is etched away. Other methods of forming the plurality of conductive traces 124 will be apparent to those skilled in the art.

As shown in FIG. 1g, a second dielectric layer 126 is disposed over the plurality of conductive traces 124 and the first dielectric layer 118. The formation of the second dielectric layer 126 may be achieved by any known process, including but not limited to film lamination, spin coating, roll coating and spray-on deposition.

As shown in FIG. 1h, a plurality of second vias 128 are then formed through the second dielectric layer 126. The plurality of second vias 128 may be formed any method known in the art, including but not limited to laser drilling and, if the second dielectric layer 126 is photoactive, forming the plurality of second vias 128 in the same manner that a photoresist mask is made in a photolithographic process, as known in the art.

If the plurality of conductive traces 124 is not capable of placing the plurality of second vias 128 in an appropriate position, then other portions of the conductive traces are formed in the plurality of second vias 128 and on the second dielectric layer 126, another dielectric layer formed thereon, and another plurality of vias is formed in the dielectric layer, such as described in FIG. 1f–1h. The layering of dielectric layers and the formation of conductive traces can be repeated until the vias are in an appropriate position. Thus, portions of a single conductive trace be formed from multiple portions thereof and can reside on different dielectric layers.

A second plurality of conductive traces 132 may be formed, wherein a portion of each of the second plurality of conductive traces 132 extends into at least one of said plurality of second vias 128. The second plurality of conductive traces 132 each include a landing pad 134 (an enlarged area on the traces demarcated by a dashed line 140), as shown in FIG. 1i.

Once the second plurality of conductive traces 132 and landing pads 134 are formed, they can be used in the formation of conductive interconnects, such as solder bumps, solder balls, pins, and the like, for communication with external components (not shown). For example, a solder mask material 136 can be disposed over the second dielectric layer 126 and the second plurality of conductive traces 132 and landing pads 134. A plurality of vias is then formed in the solder mask material 136 to expose at least a portion of each of the landing pads 134. A plurality of conductive bumps 138, such as solder bumps, can be formed, such as by screen printing solder paste followed by a reflow process or by known plating techniques, on the exposed portion of each of the landing pads 134, as shown in FIG 1j.

FIG. 2 illustrates another embodiment of the present invention wherein a plurality of microelectronic dice 102 are simultaneously encapsulated in the encapsulation material 112. The build-up layers of dielectric material and conductive element are simply represented as first build-up layer 152, second build-up layer 154, and third build-up layer 156 without illustrating the detail shown in FIGs. 1a–1j. It is, of course, understood that the microelectronic dice 102 could be encapsulated such that the microelectronic die back surfaces 114 are exposed, such that heat dissipation devices may be subsequently attached thereto, as shown in FIG. 3. Furthermore, as shown in FIG. 4, heat dissipation devices, such as heat slugs 158, could be thermally attached to the microelectronic die back surface 114, preferably with a thermally conductive adhesive (not shown), and encapsulated with the encapsulation material 112. Moreover, a microelectronic package core 150 could be utilized as a packaging material along with the encapsulation material 112 in the fabrication of the microelectronic package, such as illustrated in FIG. 5. The microelectronic package core 150 preferably comprises a substantially planar material. The material used to fabricate the microelectronic package core 150 may include, but is not limited to, a Bismaleimide Triazine ("BT") resin based material, an FR4 material (a flame retarding glass/epoxy material), and various polyimide materials. With the structures as shown in FIGs. 2-5, the individual microelectronic dice 102 are generally separated from one another in a singulation process (i.e., cutting through the encapsulation material 112 between the microelectronic dice 102 (FIGs. 2-4) or through the microelectronic package core 150 (FIG. 5)). Thus, the term "packaging material" is herein defined to include items such as the encapsulation material 112 and/or the microelectronic package core 150.

Although the build-up layer techniques described of FIGs. 1a-1j and 2-5 have many advantages, warpage induced by CTE (coefficient of thermal expansion) mismatch between the encapsulation material 112 and the dielectric layers (e.g., see dielectric layer 118 and 126 of FIGs. 1e-1i) used in the build-up layers can be significant. In general, the CTE of the dielectric layers is much larger than the CTE of the encapsulation material 112 (and microelectronic die 102). The dielectric layers are generally cured at elevated temperatures, which can result in the development of significant warpage when the assembly is cooled down. This warpage causes problems in subsequent processing steps. Thus, the following process has been developed to greatly reduce or substantially eliminate the warpage problem.

As shown in FIG. 6a, a first encapsulated die assembly 160 is provided. The first encapsulated die assembly 160 has a plurality of microelectronic dice 102 encapsulated in an encapsulation material 112 and a microelectronic package core 150 (similar to the structure shown in FIG. 5 without the build-up layers). As shown in FIG. 6b, a second encapsulated die assembly 162, which is similar to configuration of the first encapsulated die assembly 160, is attached to the first encapsulated die assembly 160. As with the first encapsulated die assembly 160, the second encapsulated die assembly 162 also has a plurality of microelectronic dice 102' encapsulated in an encapsulation material 112'. The first encapsulated die assembly 160 and the second encapsulated die assembly 162 are oriented such that the first encapsulated microelectronic die assembly back surface 130 faces the second encapsulated microelectronic die back surface 130'.

The first encapsulated die assembly 160 and the second encapsulated die assembly 162 are preferably attached together with a layer of adhesive 164. In one

embodiment, the adhesive layer 164 comprises a weak, easily removable adhesive, such as silicone- or acrylic-based material. In another embodiments, the adhesive layer 164 comprises a sol-gel material that becomes porous and brittle after drying so that debonding is achieved by fracturing the sol-gel material. In a further embodiment, the adhesive layer 164 comprises a dissolvable adhesive, wherein the adhesive dissolves in an appropriate solvent (e.g., water, alcohol, etc.). When a dissolvable adhesive is used, the adhesive layer 164 can be pattern to allow a solvent to more easily flow between the first encapsulated die assembly 160 and the second encapsulated die assembly 162 to more quickly dissolve the adhesive layer 164. FIG. 6 illustrates such a patterned adhesive layer 164 on the first encapsulated die assembly 160.

It is, of course, understood that a strong adhesive could be used as the adhesive layer 164. As shown in FIG. 8, the strong adhesive layer 164 is patterned directly in a position where a dicing saw will cut the first encapsulated die assembly 160 and the second encapsulated die assembly 162 during a subsequent singulation process. Thus, the adhesive layer 164 is also removed during the singulation process.

Referring again to FIG. 6b, once the first encapsulated die assembly 160 and the second encapsulated die assembly 162 are adhered together, build-up layers can be formed on a first encapsulated microelectronic die assembly active surface 120 and on a second encapsulated microelectronic die assembly active surface 120', as shown in FIG. 6c. The build-up layers of dielectric material and conductive element are simply represented as first build-up layer 152, second build-up layer 154, and third build-up layer 156 on the first encapsulated die assembly 160 and as first build-up layer 152', second build-up layer 154', and third build-up layer 156' without illustrating the detail

shown in FIGs. 1a–1j. It is, of course, understood that the build-up layers can be formed simultaneously on the first encapsulated die assembly 160 and the second encapsulated die assembly 162.

Due to "back-to-back" attachment of the first encapsulated die assembly 160 and the second encapsulated die assembly 162, any tendency for warpage occurring in the first encapsulated die assembly 160 will be counteracted by a substantially equal but opposite tendency for warpage occurring in the second encapsulated die assembly 162, which greatly reduces or substantially eliminates the warpage problem. Furthermore, the ability to form the build-up layers (and potentially other process steps) simultaneously improves the efficiency of microelectronic die fabrication process.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. An intermediate microelectronic package, comprising:

a first encapsulated die assembly having an active surface and a back surface, said first encapsulated die assembly including at least one first microelectronic die having an active surface and at least one side and a first packaging material adjacent said at least one first microelectronic die side; and

a second encapsulated die assembly having an active surface and a back surface, wherein said second encapsulated die assembly back surface is attached to said first encapsulated die assembly back surface, said second encapsulated die assembly including at least one second microelectronic die having an active surface and at least one side and a second packaging material adjacent said at least one second microelectronic die side.

2. The intermediate microelectronic package of claim 1, wherein said first encapsulated die assembly active surface comprises said at least one first microelectronic die active surface and at least one surface of said first packaging material which is substantially planar to said first microelectronic die active surface.

3. The intermediate microelectronic package of claim 1, wherein said second encapsulated die assembly active surface comprises said at least one second microelectronic die active surface and at least one surface of said second packaging material which is substantially planar to said first microelectronic die active surface.

4. The intermediate microelectronic package of claim 1, further including at least one layer of dielectric material disposed over said first encapsulated die assembly active surface and at least one conductive trace extending through and residing on said at least one dielectric material layer.

5. The intermediate microelectronic package of claim 1, further including at least one layer of dielectric material disposed over said second encapsulated die assembly active surface and at least one conductive trace extending through and residing on said at least one dielectric material layer.

6. The intermediate microelectronic package of claim 1, further including an adhesive material disposed between said first encapsulated die assembly back surface and second encapsulated die assembly back surface.

7. The intermediate microelectronic package of claim 6, wherein said adhesive material is disposed in a desired patterned between said first encapsulated die assembly back surface and second encapsulated die assembly back surface.

8. The intermediate microelectronic package of claim 1, wherein said first and said second packaging material comprises an encapsulation material.

9. The intermediate microelectronic package of claim 1, wherein said first and said second packaging material comprises a microelectronic package core and an encapsulation material.

10. A method of fabricating microelectronic dice, comprising:

providing a first encapsulated die assembly having an active surface and a back surface, said first encapsulated die assembly including at least one first microelectronic die having an active surface and at least one side and a first packaging material adjacent said at least one first microelectronic die side; and

providing a second encapsulated die assembly having an active surface and a back surface, said second encapsulated die assembly including at least one second microelectronic die having an active surface and at least one side and a second packaging material adjacent said at least one second microelectronic die side; and

attaching said first encapsulated die assembly back surface to said second encapsulated assembly back surface.

11. The method of claim 10, further including forming at least one layer of dielectric material over said first encapsulated die assembly active surface.

12. The method of claim 11, further including forming at least one conductive trace extending through and residing on said at least one dielectric material layer.

13. The method of claim 10, further including forming at least one layer of dielectric material over said second encapsulated die assembly active surface.

14. The method of claim 13, further including forming at least one conductive trace extending through and residing on said at least one dielectric material layer.

15. The method of claim 10, further including simultaneously forming at least one layer of dielectric material over said first encapsulated die assembly active surface and at least one layer of dielectric material over said second encapsulated die assembly active surface.

16. The method of claim 15, further including simultaneously forming at least one conductive trace extending through and residing on said at least one dielectric material layer on said first encapsulated die assembly and at least one conductive trace extending through and residing on said at least one dielectric material layer on said second encapsulated die assembly.

17. The method of claim 10, wherein said attaching said first encapsulated die assembly back surface to said second encapsulated assembly back surface comprises disposing an adhesive on said first encapsulated die assembly back surface and contacting said second encapsulated assembly back surface with said adhesive.

18. The method of claim 17, wherein said disposing an adhesive on said first encapsulated die assembly back surface comprises patterning said adhesive on said first encapsulated die assembly back surface.

19. The method of claim 18, wherein said patterning said adhesive comprises placing at least one adhesive line between a first microelectronic die and an adjacent microelectronic die on said first encapsulated die assembly back surface.

20. The method of claim 19, further including dicing said first encapsulated die assembly and said second encapsulated die assembly such that said dicing removes said at least one adhesive line.

21. The method of claim 10, wherein said providing a first encapsulated die assembly comprises:

providing at least one first microelectronic die having an active surface and at least one side;

abutting a protective film against said at least one first microelectronic die active surface;

encapsulating said at least one microelectronic die with an encapsulation material adjacent said at least one first microelectronic die side, wherein said encapsulation material provides at least one surface of said encapsulation material substantially planar to said first microelectronic die active surface; and

removing said protective film.

22. The method of claim 10, wherein said providing a second encapsulated die assembly comprises:

providing at least one second microelectronic die having an active surface and at least one side;

abutting a protective film against said at least one second microelectronic die active surface;

encapsulating said at least one microelectronic die with an encapsulation material adjacent said at least one second microelectronic die side, wherein said encapsulation material provides at least one surface of said encapsulation material substantially planar to said second microelectronic die active surface; and

removing said protective film.

23. A method of fabricating a microelectronic package, comprising:

forming a first encapsulated die assembly comprising:

providing at least one first microelectronic die having an active surface and at least one side;

abutting a protective film against said at least one first microelectronic die active surface; and

encapsulating said at least one microelectronic die with an packaging material adjacent said at least one first microelectronic die side

to form a first encapsulated die active surface and a first encapsulated die back surface;

forming a second encapsulated die assembly comprising:

providing at least one second microelectronic die having an active surface and at least one side;

abutting a protective film against said at least one second microelectronic die active surface; and

encapsulating said at least one microelectronic die with an packaging material adjacent said at least one second microelectronic die side to form a second encapsulated die active surface and a second encapsulated die back surface; and

attaching said first encapsulated die assembly back surface to said second encapsulated assembly back surface.

24. The method of claim 23, further including forming at least one layer of dielectric material over said first encapsulated die assembly active surface.

25. The method of claim 23, further including forming at least one conductive trace extending through and residing on said at least one dielectric material layer.

26. The method of claim 23, further including forming at least one layer of dielectric material over said second encapsulated die assembly active surface.

27. The method of claim 23, further including forming at least one conductive trace extending through and residing on said at least one dielectric material layer.

28. The method of claim 23, further including simultaneously forming at least one layer of dielectric material over said first encapsulated die assembly active surface and at least one layer of dielectric material over said second encapsulated die assembly active surface.

29. The method of claim 28, further including simultaneously forming at least one conductive trace extending through and residing on said at least one dielectric material layer on said first encapsulated die assembly and at least one conductive trace extending through and residing on said at least one dielectric material layer on said second encapsulated die assembly.

30. The method of claim 23, wherein said attaching said first encapsulated die assembly back surface to said second encapsulated assembly back surface comprises disposing an adhesive on said first encapsulated die assembly back surface and contacting said second encapsulated assembly back surface with said adhesive.

31. The method of claim 30, wherein said disposing an adhesive on said first encapsulated die assembly back surface comprises patterning said adhesive on said first encapsulated die assembly back surface.

32. The method of claim 31, wherein said patterning said adhesive comprises placing at least one adhesive line between a first microelectronic die and an adjacent microelectronic die on said first encapsulated die assembly back surface.

33. The method of claim 32, further including dicing said first encapsulated die assembly and said second encapsulated die assembly such that said dicing removes said at least one adhesive line.

ABSTRACT OF DISCLOSURE

A method of fabricating microelectronic dice by providing or forming a first encapsulated die assembly and a second encapsulated die assembly. Each of the encapsulated die assemblies includes at least one microelectronic die disposed in a packaging material. Each of the encapsulated die assemblies has an active surface and a back surface. The encapsulated die assemblies are attached together in a back surface-to-back surface arrangement. Build-up layers are then formed on the active surfaces of the first and second encapsulated assemblies, preferably, simultaneously. Thereafter, the microelectronic dice are singulated, if required, and the microelectronic dice of the first encapsulated die assembly are separated from the microelectronic dice of the second encapsulated die assembly.

FIG. 1a

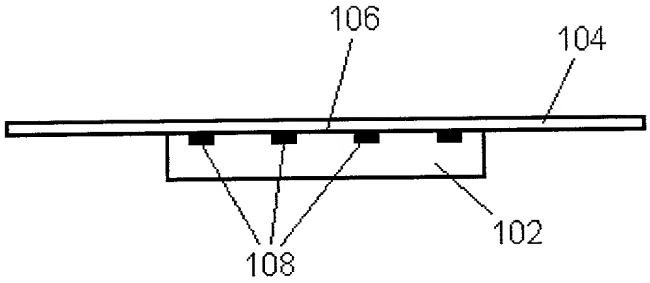

FIG. 1b

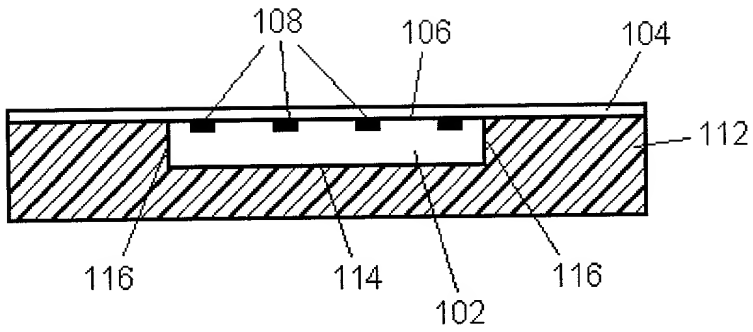

FIG. 1c

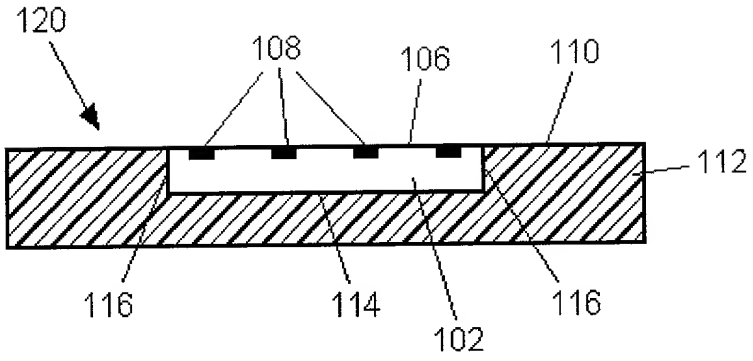

FIG. 1d

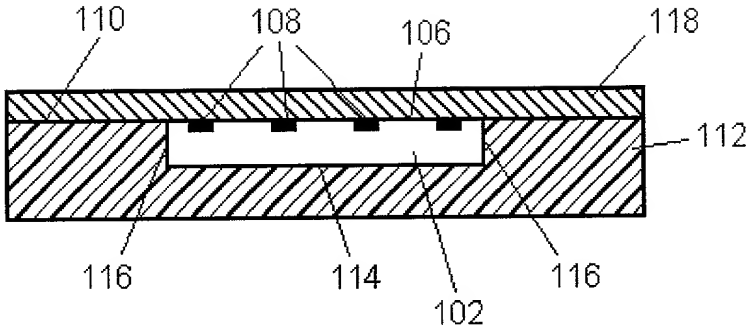

FIG. 1e

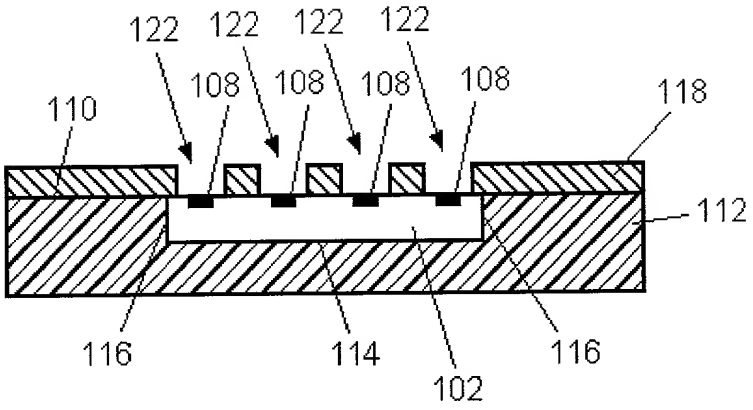

FIG. 1f

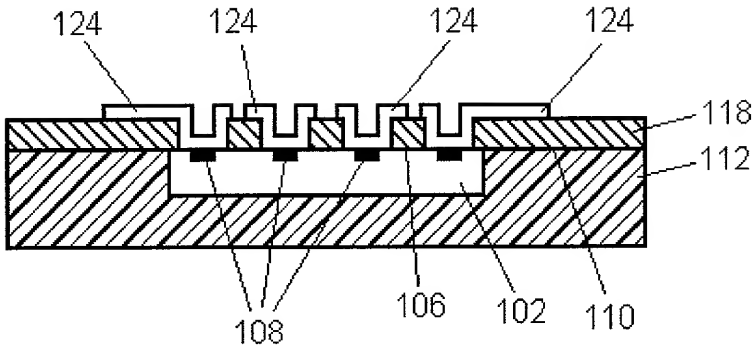

FIG. 1g

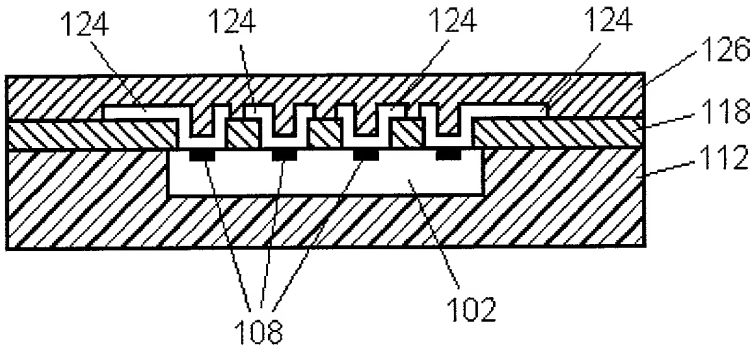

FIG. 1h

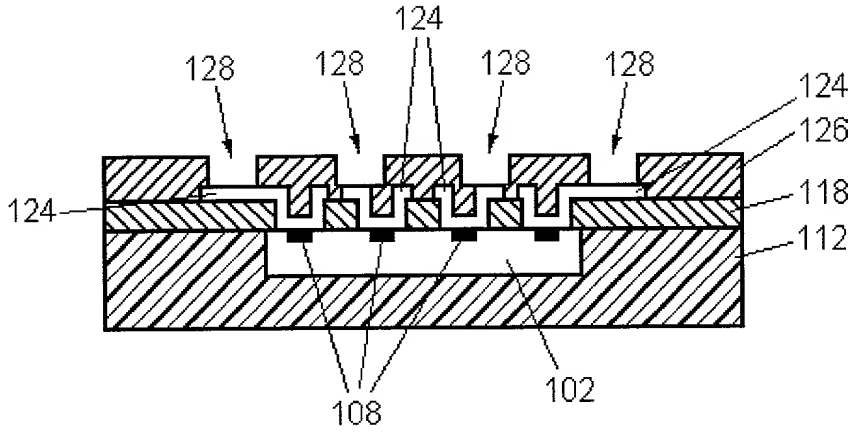

FIG. 1i

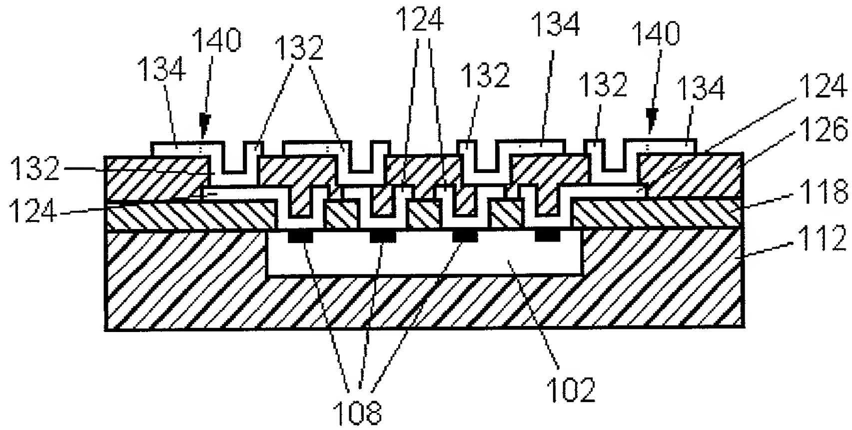
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FIG. 1j

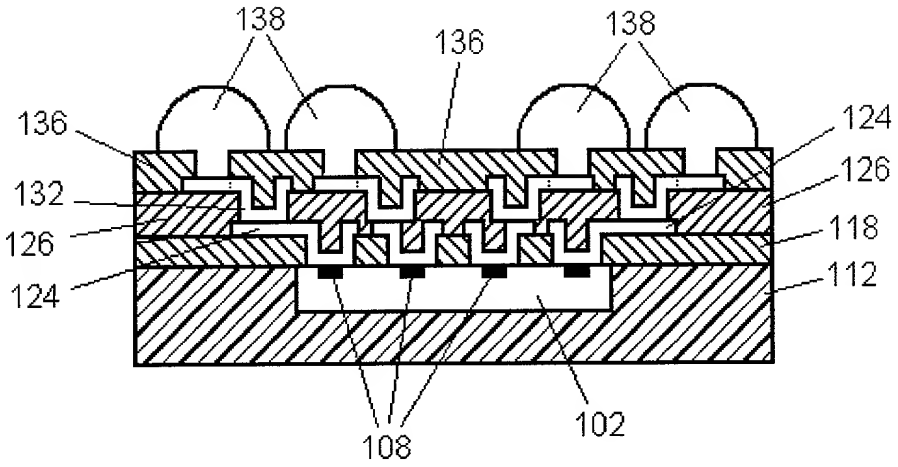

FIG. 2

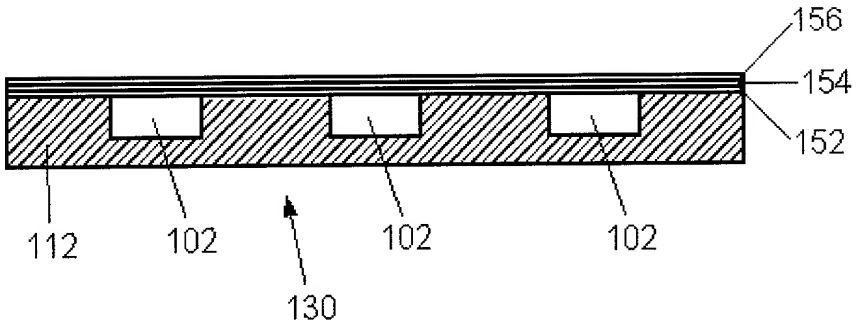

FIG. 3

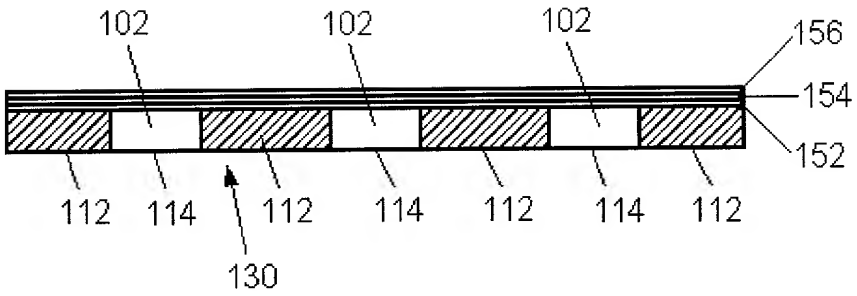

FIG. 4

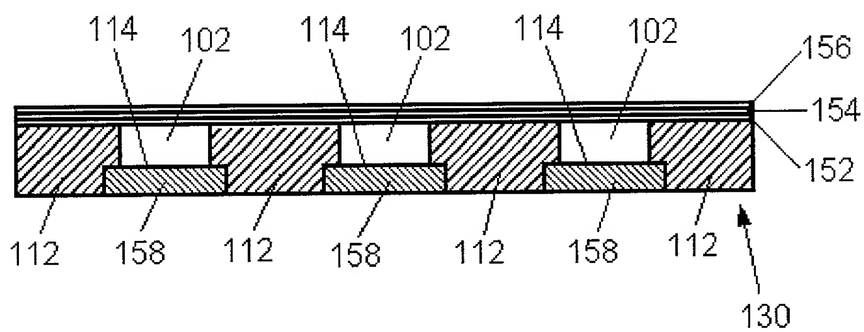
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FIG. 5

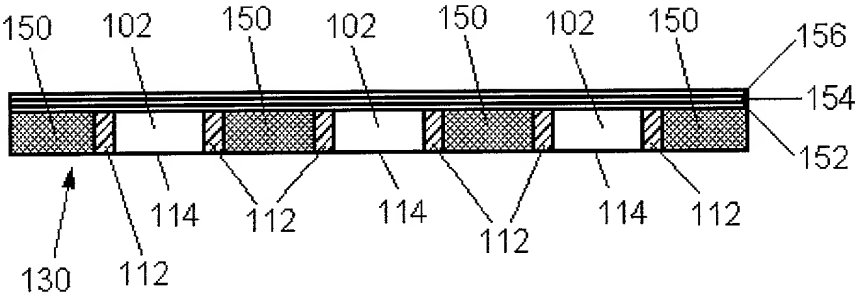
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FIG. 6a

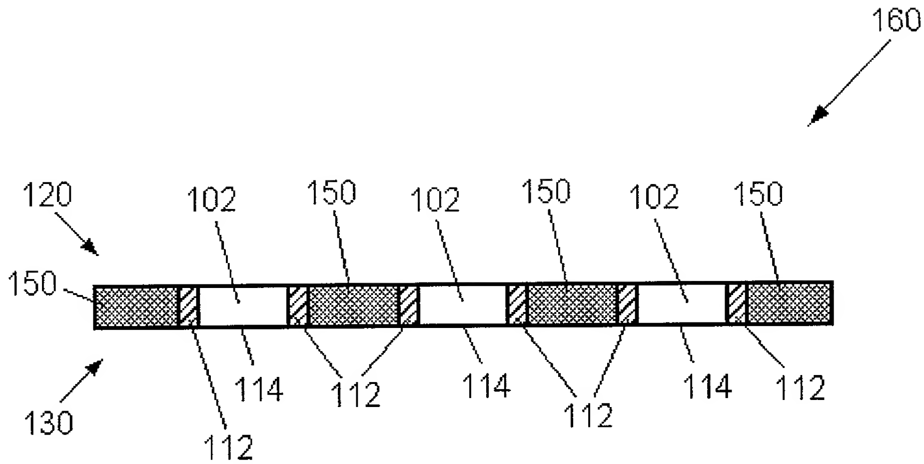
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FIG. 6b

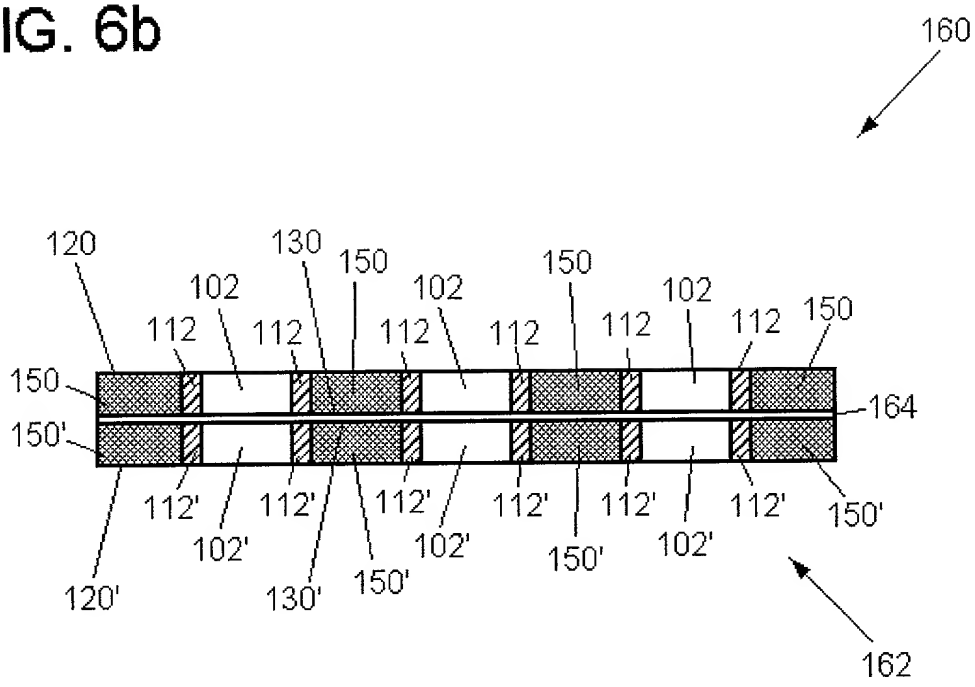

FIG. 6c

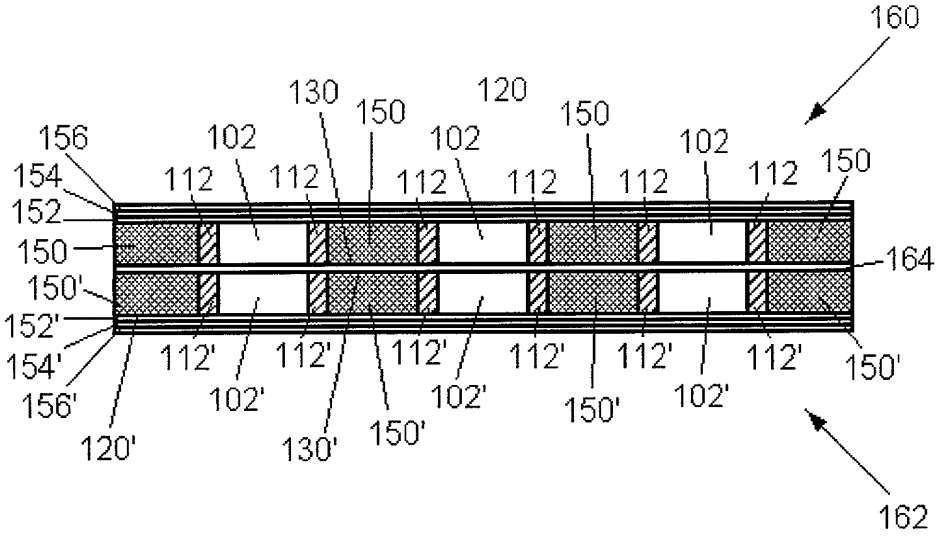
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FIG. 7

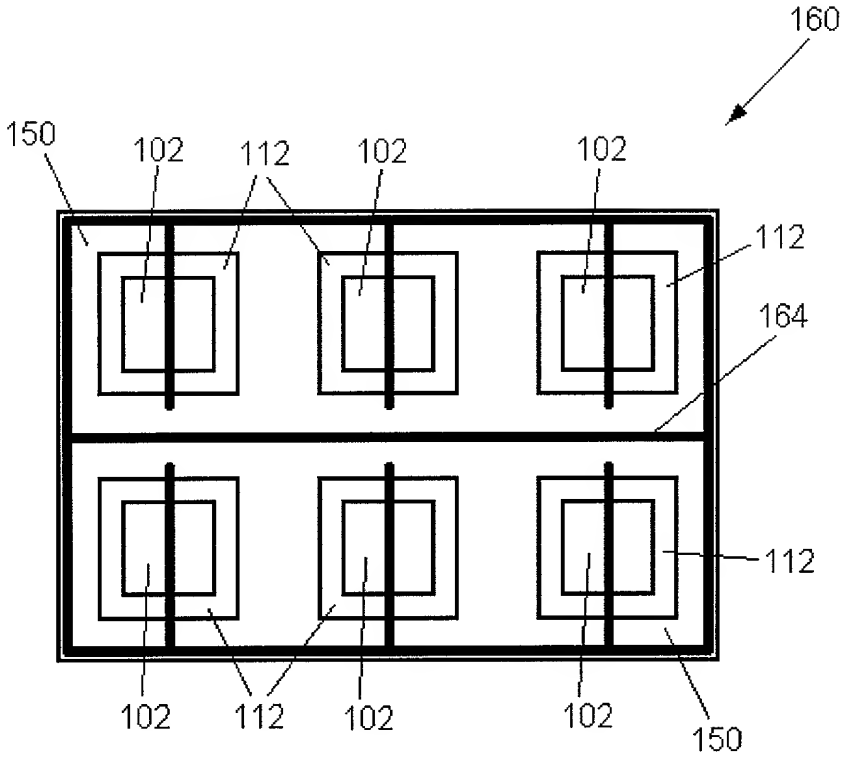


FIG. 8

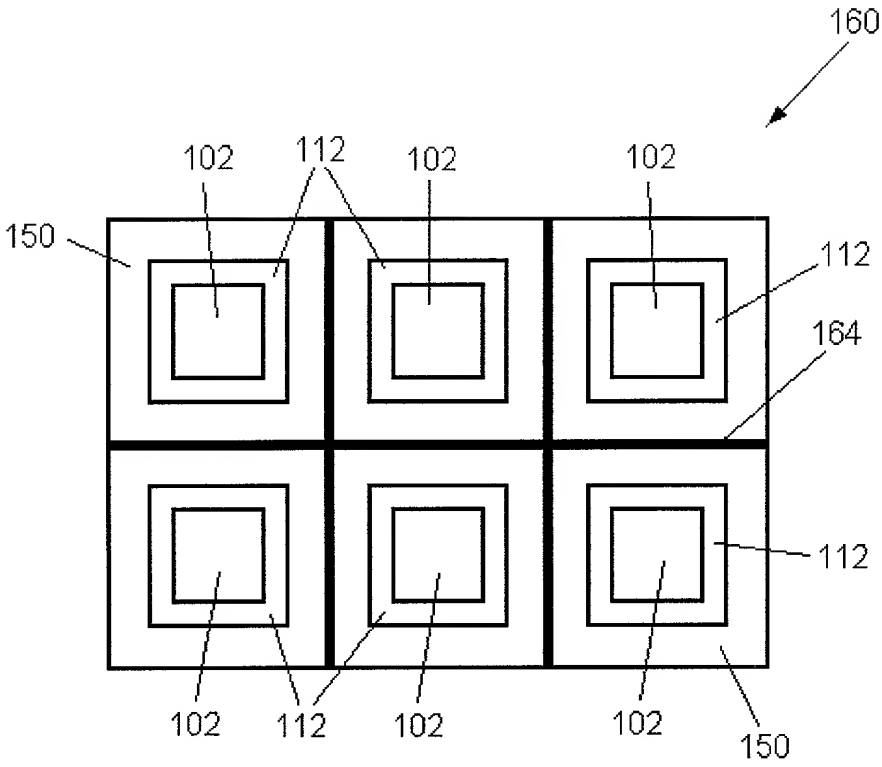


FIG. 9
PRIOR ART

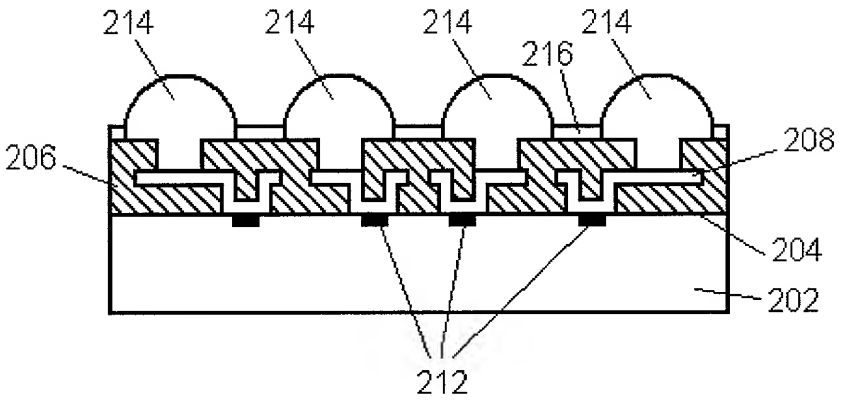


FIG. 10
PRIOR ART

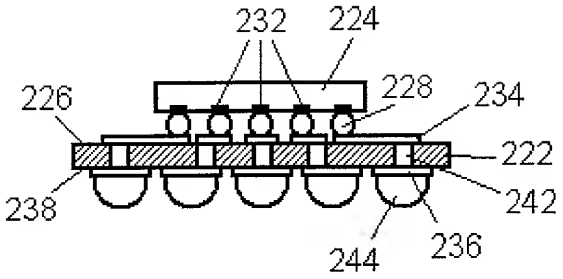
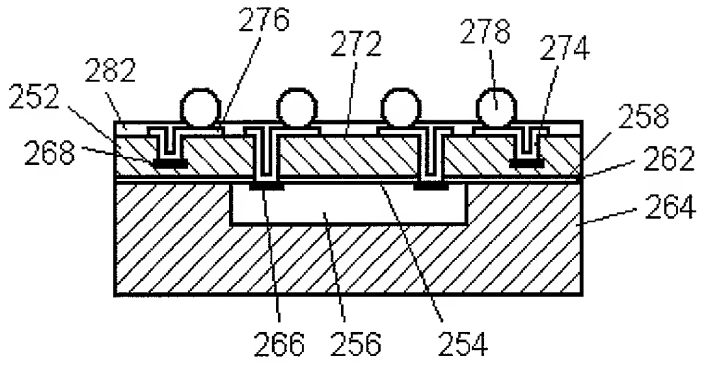


FIG. 11
PRIOR ART



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PROCESS FOR FORMING A DIRECT BUILD-UP LAYER ON AN ENCAPSULATED DIE PACKAGE AND INTERMEDIATE STRUCTURES FORMED THEREWITH

the specification of which

☒ is attached hereto.
☐ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____ (if applicable).

☐ I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

☐ I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

☐ I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to:
Robert G. Winkle, Reg. No. 37,474, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
(Name of Attorney or Agent)
12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to:
Robert G. Winkle, (503) 684-6200.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name) **Chun Mu**

Inventor's Signature _____ Date _____

Residence Saratoga, California USA Citizenship USA
(City, State) *(Country)*

P. O. Address 19685 Via Escuela Drive

Saratoga, California 95070 USA

Full Name of Second/Joint Inventor (given name, family name) **Qing Ma**

Inventor's Signature _____ Date _____

Residence San Jose, California USA Citizenship USA
(City, State) *(Country)*

P. O. Address 919 Brentwood Drive

San Jose, California 95129 USA

Full Name of Third/Joint Inventor (given name, family name) **Quat Vu**

Inventor's Signature _____ Date _____

Residence Santa Clara, California USA Citizenship USA
(City, State) *(Country)*

P. O. Address 3065 Bowers Avenue

Santa Clara, California 95052 USA

Full Name of Fourth/Joint Inventor (given name, family name) **Steven Towle**

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) *(Country)*

P. O. Address _____

_____

Full Name of Fifth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) *(Country)*

P. O. Address _____

_____

APPENDIX A

William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Lisa N. Benado, Reg. No. 39,995; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; R. Alan Burnett, Reg. No. 46,149; Gregory D. Caldwell, Reg. No. 39,926; Andrew C. Chen, Reg. No. 43,544; Thomas M. Coester, Reg. No. 39,637; Donna Jo Coningsby, Reg. No. 41,684; Florin Corie, Reg. No. 46,244; Dennis M. deGuzman, Reg. No. 41,702; Stephen M. De Klerk, Reg. No. P46,503; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Sanjeet Dutta, Reg. No. P46,145; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; George Fountain, Reg. No. 37,374; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Sang Hui Kim, Reg. No. 40,450; Walter T. Kim, Reg. No. 42,731; Eric T. King, Reg. No. 44,188; Erica W. Kuo, Reg. No. 42,775; George B. Leavell, Reg. No. 45,436; Gordon R. Lindeen III, Reg. No. 33,192; Jan Carol Little, Reg. No. 41,181; Kurt P. Leyendecker, Reg. No. 42,799; Joseph Lutz, Reg. No. 43,765; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Clive D. Menezes, Reg. No. 45,493; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Daniel E. Ovanezian, Reg. No. 41,236; Kenneth B. Paley, Reg. No. 38,989; Gregg A. Peacock, Reg. No. 45,001; Marina Portnova, Reg. No. P45,750; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; Joseph A. Twarowski, Reg. No. 42,191; Thomas A. Van Zandt, Reg. No. 43,219; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. P46,322; Thomas C. Webster, Reg. No. P46,154; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Justin M. Dillon, Reg. No. 42,486; my patent agent, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; John N. Greaves, Reg. No. 40,362; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; Steven D. Yates, Reg. No. 42,242, and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. 44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.